Low-Noise Clock Jitter Cleaner with Dual Loop PLLs

1.0 General Description

The LMK04820 family is the industry's highest performance clock conditioner with JEDEC JESD204B support. The dual loop PLLatinum™ architecture enables sub-100 fs RMS jitter (10 kHz to 20 MHz) using a low noise VCXO module.

The dual loop architecture consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO). The first PLL (PLL1) provides a low-noise jitter cleaner function while the second PLL (PLL2) performs the clock and SYSREF generation. PLL1 can be configured to either work with an external VCXO module or the integrated crystal oscillator with an external tunable crystal and varactor diode. When used with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module or tunable crystal used in PLL1.

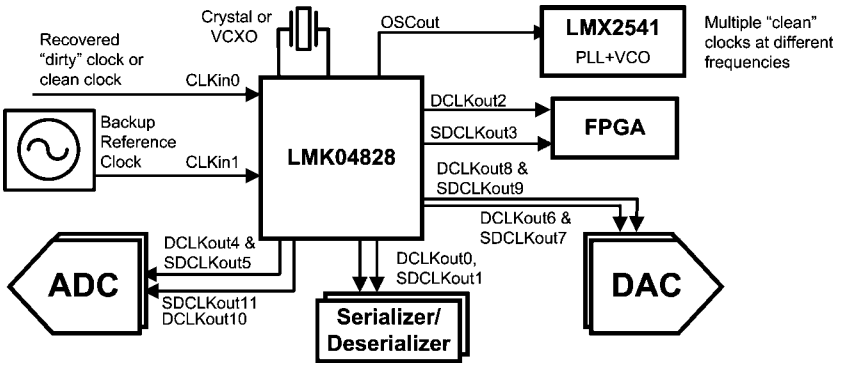
Device	VCO1 Frequency	VCO2 Frequency
LMK04828	2370 to 2600 MHz	2945 to 3005 MHz
LMK04826	1785 to 1970 MHz	2455 to 2505 MHz

2.0 Target Applications

- JEDEC JESD204B
- Wireless Infrastructure
- Data Converter Clocking
- Networking, SONET/SDH, DSLAM
- Medical / Video / Military / Aerospace
- Test and Measurement

3.0 Features

- JEDEC JESD204B Support
  - 7 Device clocks and up to 7 SYSREF Clocks
  - Up to 14 Differential Device Clocks
  - LVPECL, LVDS, or HSDS programmable outputs
- Ultra-Low RMS Jitter Performance
- Dual Loop PLLatinum PLL Architecture
  - PLL1
    - Integrated Low-Noise Crystal Oscillator Circuit
    - Holdover mode when input clocks are lost
      - Automatic or manual triggering/recovery
    - Hitless switching mode
  - PLL2
    - Normalized [1 Hz] PLL noise floor of -227 dBc/Hz
    - Phase detector rate up to 155 MHz
    - OSCin frequency-doubler
    - Two Integrated Low-Noise VCOs
- 2 redundant input clocks with LOS
  - Automatic and manual switch-over modes
  - Hitless switching
- 50% duty cycle output divides, 1 to 32 (even and odd)
- Precision digital delay, fixed or dynamically adjustable
- 25 ps step analog delay.
- 0-delay mode
- Multi-mode: Dual PLL, single PLL, and clock distribution
- Industrial Temperature Range: -40 to 85 °C
- 3.15 V to 3.45 V operation
- Package: 64-pin LLP (9.0 x 9.0 x 0.8 mm)



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4.0 Device Configuration Information

NSID	Reference Inputs	Dedicated Buffered/Divided OSCin Clock LVDS/ LVPECL/LVCMOS	Programmable LVDS/LVPECL/ HSDS Outputs	VCO1 Frequency	VCO2 Frequency
LMK04828BISQ	2	1	14	2370 to 2600 MHz	2945 to 3005 MHz
LMK04826BISQ	2	1	14	1785 to 1970 MHz	2455 to 2505 MHz

5.0 Functional Block Diagrams and Operating Modes

The LMK04820 Family is a flexible device that can be configured for many different use cases. The following simplified block diagrams help show the user the different use cases of the device.

5.1 Dual PLL

Figure 1 illustrates the typical use case of the LMK04820 in dual loop mode. In dual loop mode the reference to PLL1 is either CLKin0 or CLKin1. An external VCXO or tunable crystal will be used to provide feedback for the first PLL and a reference to the second PLL. This first PLL cleans the jitter with the VCXO or low cost tunable crystal by using a narrow loop bandwidth. The VCXO or tunable crystal output may be buffered through the OSCout port and optionally on up to 4 of the CLKouts. The VCXO or tunable crystal is used as the reference to PLL2 and may be doubled using the frequency doubler. The internal VCO drives up to six divide/ delay blocks which drive up to 14 clock outputs. The eighth divider/delay block is creating the SYSREF frequency.

Hitless switching and holdover functionality are optionally available when the input reference clock is lost. Holdover works by fixing the tuning voltage of PLL1 to the VCXO or tunable crystal.

It is also possible to use an external VCO in place of PLL2's internal VCO. In this case one less CLKin is available as a reference.

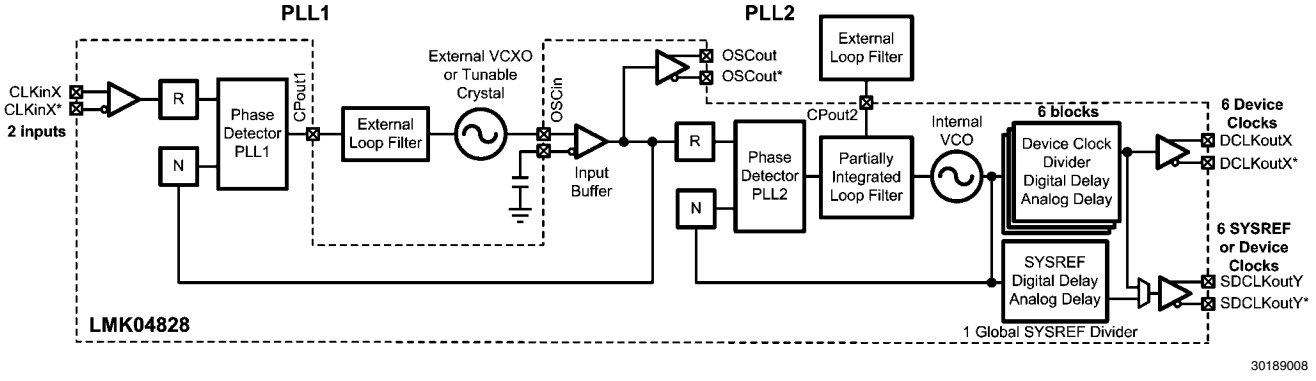

FIGURE 1. Simplified Functional Block Diagram for Dual Loop Mode

5.2 0-Delay Dual PLL

Figure 2 illustrates the use case of cascaded 0-delay dual loop mode. This configuration differs from *Figure 1* in that the feedback for PLL2 is driven by a clock output instead of the VCO output.

It is also possible to use an external VCO in place of PLL2's internal VCO; but one less CLKin is available as a reference.

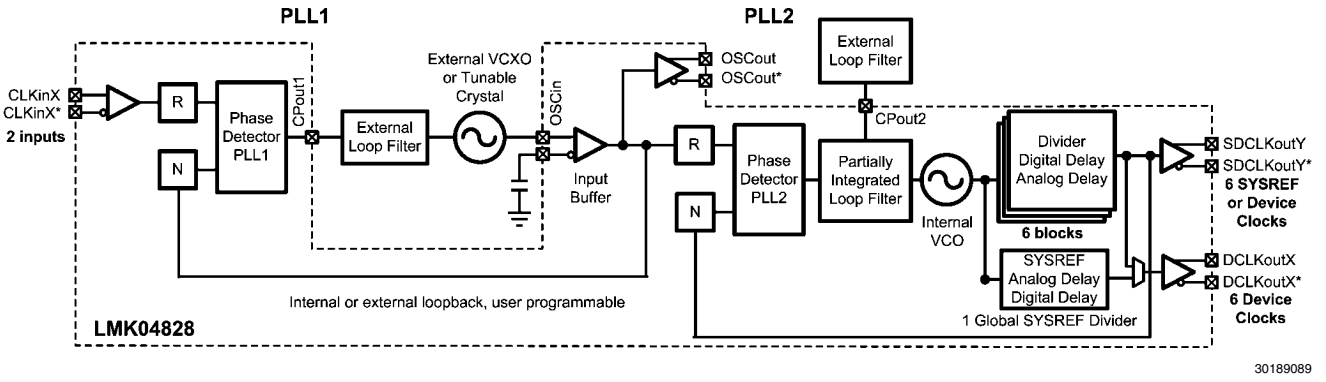

FIGURE 2. Simplified Functional Block Diagram for Cascaded 0-delay Dual Loop Mode

illustrates the use case of nested 0-delay dual loop mode. This configuration is similar to except that the feedback to the first PLL is driven by a clock output. This causes the clock outputs to have deterministic phase with the clock input. Since all the clock outputs can be synchronized together, all the clock outputs can be in phase with the clock input signal. The feedback to PLL1 can be connected internally as shown, or externally using FBCLKin (CLKin1) as an input port.

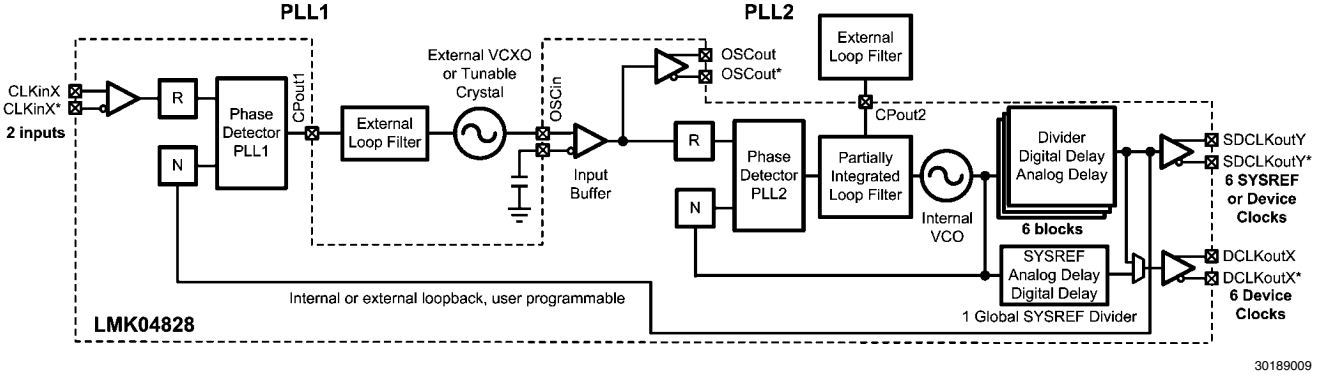

FIGURE 3. Simplified Functional Block Diagram for Nested 0-delay Dual Loop Mode

5.3 Detailed LMK04820 Family Block Diagram

Figure 4 illustrates the complete LMK04820 family block diagram.

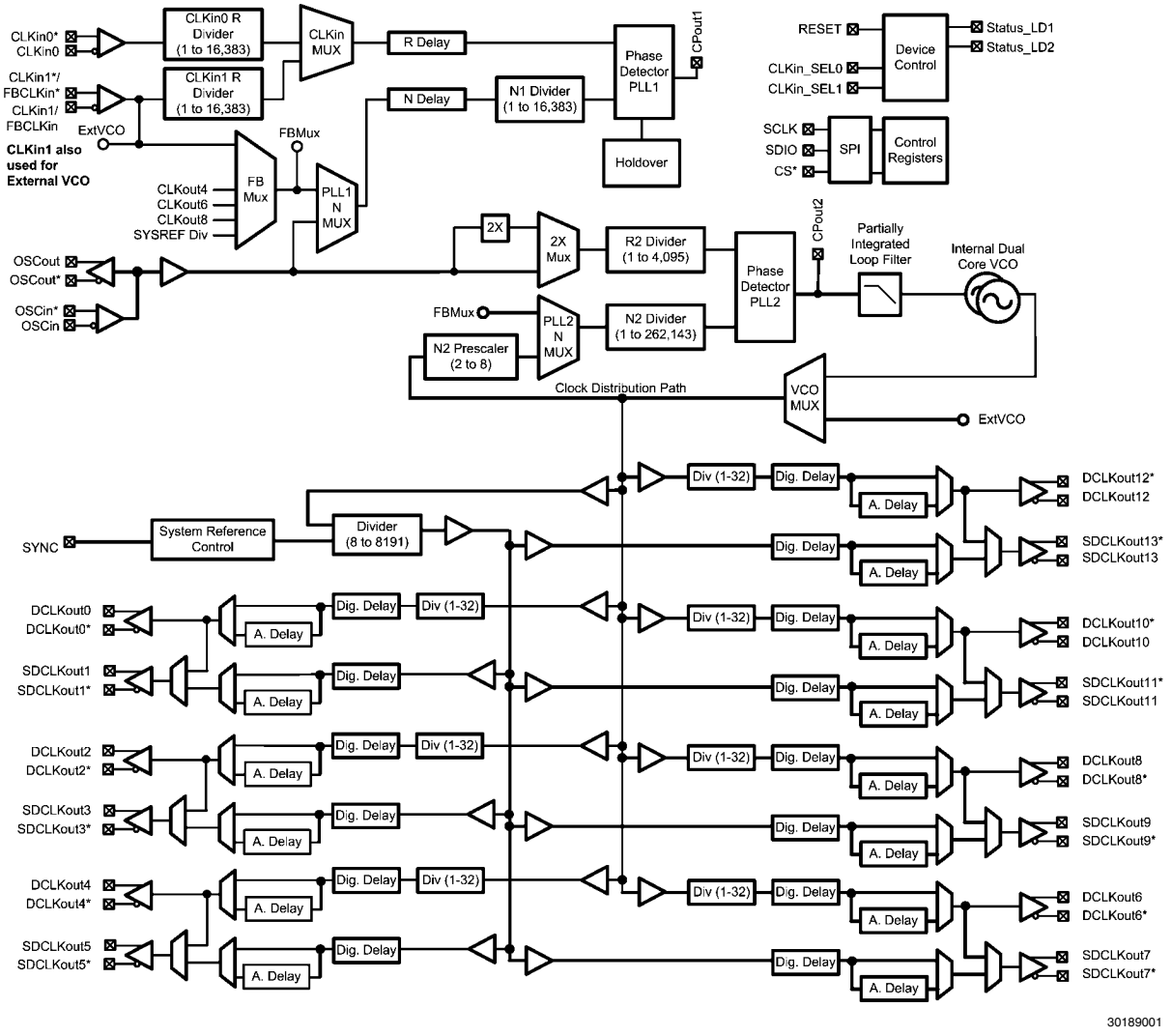

FIGURE 4. Detailed LMK04820 Family Block Diagram

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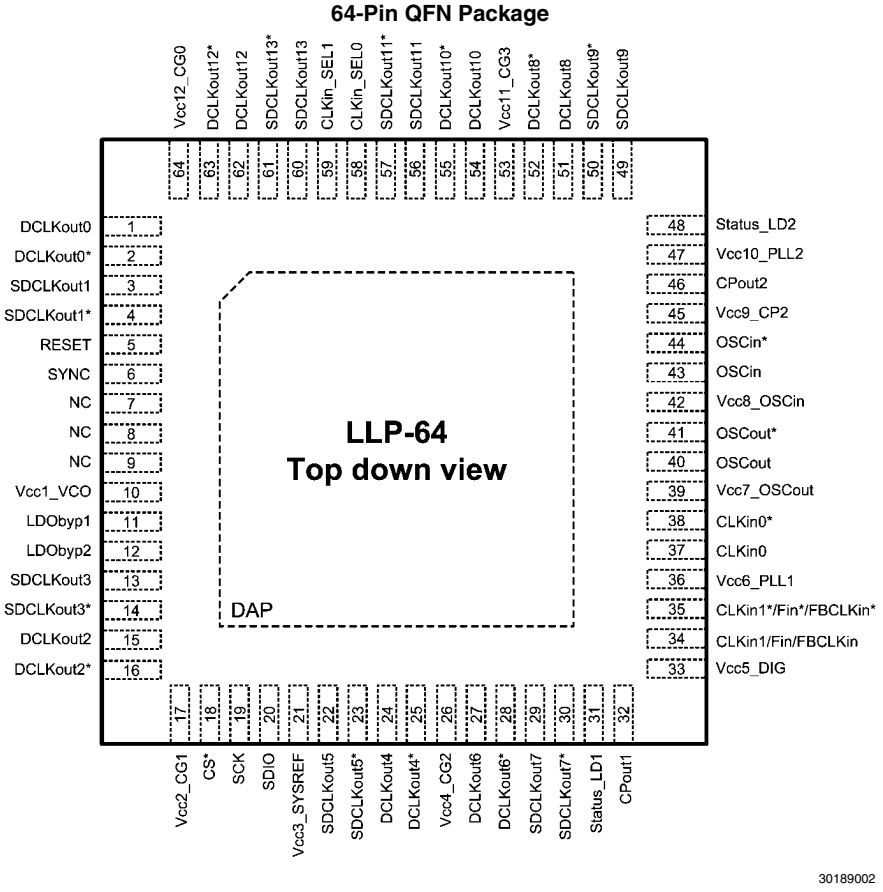
6.0 Connection Diagram



7.0 Pin Descriptions

Pin Number	Name(s)	I/O	Type	Description
1, 2	DCLKout0, DCLKout0*	O	Programmable	Device clock output 0.
3, 4	SDCLKout1, SDCLKout1*	O	Programmable	SYSREF / Device clock output 1
5	RESET	I/O	ANLG	Device reset input.
6	SYNC	I/O	CMOS	Synchronization input or programmable status pin.
7, 8, 9	NC			No Connection. These pins must be left floating.
10	Vcc1_VCO		PWR	Power supply for VCO LDO.
11	LDObyp1		ANLG	LDO Bypass, bypassed to ground with 10 µF capacitor.
12	LDObyp2		ANLG	LDO Bypass, bypassed to ground with a 0.1 µF capacitor.
13, 14	SDCLKout3, SDCLKout3*	O	Programmable	SYSREF / Device Clock output 3.
15, 16	DCLKout2, DCLKout2*	O	Programmable	Device clock output 2.
17	Vcc2_CG1		PWR	Power supply for clock outputs 2 and 3.
18	CS*	I	CMOS	Chip Select, active low.
19	SCK	I	CMOS	SPI Clock
20	SDIO	I/O	CMOS	SPI Data
21	Vcc3_SYSREF		PWR	Power supply for SYSREF divider and SYNC.
22, 23	SDCLKout5, SDCLKout5*	O	Programmable	SYSREF / Device clock output 5.
24, 25	DCLKout4, DCLKout4*	O	Programmable	Device clock output 4.
26	Vcc4_CG2		PWR	Power supply for clock outputs 4, 5, 6 and 7.
27, 28	DCLKout6, DCLKout6*	O	Programmable	Device clock output 6.
29, 30	SDCLKout7, SDCLKout7*	O	Programmable	SYSREF / Device clock output 7.
31	Status_LD1	I/O	Programmable	Programmable status pin.
32	CPout1	O	ANLG	Charge pump 1 output.
33	Vcc5_DIG		PWR	Power supply for the digital circuitry.
34, 35	CLKin1, CLKin1*	I	ANLG	Reference Clock Input Port for PLL1, AC or DC Coupled
	FBCLKin, FBCLKin*	I	ANLG	Feedback input for external clock feedback input (0–delay mode). AC or DC coupled.
	Fin, Fin*	I	ANLG	External VCO Input (External VCO mode). AC or DC coupled.
36	Vcc6_PLL1		PWR	Power supply for PLL1, charge pump 1.
37, 38	CLKin0, CLKin0*	I	ANLG	Reference Clock Input Port 0 for PLL1. AC or DC coupled.
39	Vcc7_OSCout		PWR	Power supply for OSCout port.
40,41	OSCout, OSCout*	O	Programmable	Buffered output of OSCin port.
42	Vcc8_OSCin		PWR	Power supply for OSCin
43, 44	OSCin, OSCin*	I	ANLG	Feedback to PLL1, Referenc input to PLL2. AC coupled.
45	Vcc9_CP2		PWR	Power supply for PLL2 Charge Pump.
46	CPout2	O	ANLG	Charge pump 2 output.
47	Vcc10_PLL2		PWR	Power supply for PLL2.

Pin Number	Name(s)	I/O	Type	Description
48	Status_LD2	I/O	Programmable	Programmable status pin.
49, 50	SDCLKout9, SDCLKout9*	O	Programmable	SYSREF / Device clock 9
51, 52	DCLKout8, DCLKout8*	O	Programmable	Device clock output 8.
53	Vcc11_CG3		PWR	Power supply for clock outputs 8, 9, 10, and 11.
54, 55	DCLKout10, DCLKout10*	O	Programmable	Device clock output 10.
56, 57	SDCLKout11, SDCLKout11*	O	Programmable	SYSREF / Device clock output 11.
58	CLKin_SEL0	I/O	Programmable	Programmable status pin.
59	CLKin_SEL1	I/O	Programmable	Programmable status pin.
60, 61	SDCLKout13, SDCLKout13*	O	Programmable	SYREF / Device clock output 13.
62, 63	DCLKout12, DCLKout12*	O	Programmable	Device clock output 12.
64	Vcc12_CG0		PWR	Power supply for clock outputs 0, 1, 12, and 13.
DAP	DAP		GND	DIE ATTACH PAD, connect to GND.

8.0 Absolute Maximum Ratings (Note 1, Note 2, Note 3)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Supply Voltage (Note 4)	V_{CC}	-0.3 to 3.6	V
Input Voltage	V_{IN}	-0.3 to (V_{CC} + 0.3)	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4 seconds)	T_L	+260	°C
Junction Temperature	T_J	150	°C
Differential Input Current (CLKinX/X*, OSCin/OSCin*, FBCLKin/FBCLKin*, Fin/Fin*)	I_{IN}	± 5	mA
Moisture Sensitivity Level	MSL	3	

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only to the test conditions listed.

Note 2: This device is a high performance RF integrated circuit with an ESD rating up to 2 kV Human Body Model, up to 150 V Machine Model, and up to 750 V Charged Device Model and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.

Note 3: Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is only implied at these or any other conditions in excess of those given in the operation sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Note 4: Never to exceed 3.6 V.

9.0 Package Thermal Resistance

64-Pin QFN

Parameter	Symbol	Ratings	Units
Thermal resistance from junction to ambient on 4-layer JEDEC PCB (Note 5)	θ_{JA}	TBD	° C/W
Thermal resistance from junction to case (Note 6)	θ_{JC}	TBD	° C/W

Note 5: Specification assumes 32 thermal vias connect the die attach pad to the embedded copper plane on the 4-layer JEDEC PCB. These vias play a key role in improving the thermal performance of the QFN. Note that the JEDEC PCB is a standard thermal measurement PCB and does not represent best performance a PCB can achieve. It is recommended that the maximum number of vias be used in the board layout. θ_{JA} is unique for each PCB.

Note 6: Case is defined as the DAP (die attach pad).

10.0 Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Junction Temperature	T_J				125	°C
Ambient Temperature	T_A	V_{CC} = 3.3 V	-40	25	85	°C
Supply Voltage	V_{CC}		3.15	3.3	3.45	V

11.0 Features

11.1 JITTER CLEANING

The dual loop PLL architecture of the LMK04820 family provides the lowest jitter performance over the widest range of output frequencies and phase noise integration bandwidths. The first stage PLL (PLL1) is driven by an external reference clock and uses an external VCXO or tunable crystal to provide a frequency accurate, low phase noise reference clock for the second stage frequency multiplication PLL (PLL2). PLL1 typically uses a narrow loop bandwidth (10 Hz to 200 Hz) to retain the frequency accuracy of the reference clock input signal while at the same time suppressing the higher offset frequency phase noise that the reference clock may have accumulated along its path or from other circuits. This “cleaned” reference clock provides the reference input to PLL2.

The low phase noise reference provided to PLL2 allows PLL2 to operate with a wide loop bandwidth (50 kHz to 200 kHz). The loop bandwidth for PLL2 is chosen to take advantage of the superior high offset frequency phase noise profile of the internal VCO and the good low offset frequency phase noise of the reference VCXO or tunable crystal.

Ultra low jitter is achieved by allowing the external VCXO or Crystal's phase noise to dominate the final output phase noise at low offset frequencies and the internal VCO's phase noise to dominate the final output phase noise at high offset frequencies. This results in best overall phase noise and jitter performance.

11.2 JEDEC JESD204B

The LMK04820 family provides support for JEDEC JESD204B. There are 7 outputs (SDCLKoutY) that can be configured as SYSREF outputs. These outputs are grouped with a device clock (DCLKoutX) to provide the device clock / SYSREF pair. The SYSREF clocks output LVDS, LVPECL, and HSDS formats. The SYSREF clock is generated from clock distribution path signal that has a large divider (8 to 8191) to generate the pulsed or continuous SYSREF outputs. The SYSREF also has digital and analog delay capabilities for each individual SYSREF output.

11.3 PLL1 REDUNDANT REFERENCE INPUTS (CLKin0/CLKin0* and CLKin1/CLKin1*)

The LMK04820 has two reference clock inputs for PLL1, CLKin0 and CLKin1, the active clock is chosen based on CLKin_SEL_MODE programming field. Automatic or manual switching can occur between the inputs.

CLKin0 and CLKin1 each have input dividers. The clock input divider is used as a PLL1 reference divider for each input separately. This allows flexibility for the user when switching between two different reference frequencies.

CLKin1 is shared for use as an external 0-delay feedback (FBCLKin), or for use with an external VCO (Fin).

Fast manual switching between reference clocks is possible with a external pins CLKin_SEL0 and CLKin_SEL1.

11.4 VCXO/CRYSTAL BUFFERED OUTPUT

The LMK04820 provides 1 dedicated output which is a buffered copy of the PLL2 reference input. This reference input is typically a low noise VCXO or Crystal. When using a VCXO, this output can be used to clock external devices such as microcontrollers, FPGAs, CPLDs, etc. before the LMK04828 is programmed.

The OSCout buffer output type is programmable to LVDS, LVPECL, or LVCMOS.

11.5 FREQUENCY HOLDOVER

The LMK04820 supports holdover operation to keep the clock outputs on frequency with minimum drift when the reference is lost until a valid reference clock signal is re-established.

11.6 PLL2 INTEGRATED LOOP FILTER POLES

The LMK04820 features programmable 3rd and 4th order loop filter poles for PLL2. These internal resistors and capacitor values may be selected from a fixed range of values to achieve either a 3rd or 4th order loop filter response. The integrated programmable resistors and capacitors compliment external components mounted near the chip.

These integrated components can be effectively disabled by programming the integrated resistors and capacitors to their minimum values.

11.7 INTERNAL VCOs

The LMK04820 has two internal VCOs, selected by VCO_MUX. The output of the selected VCO is routed to the Clock Distribution Path. This same selection is also fed back to the PLL2 phase detector through a prescaler and N-divider.

11.8 EXTERNAL VCO MODE

The Fin/Fin* input allows an external VCO to be used with PLL2 of the LMK04820.

Using an external VCO reduces the number of available clock inputs by one and prevents use of external 0–delay feedback.

11.9 CLOCK DISTRIBUTION

The LMK04820 features a total of 14 outputs driven from the internal or external VCO.

All VCO driven outputs have programmable output types. They can be programmed to LVPECL, LVDS, or HSDS.

If the buffered OSCin output, OSCout, is included in the total number of clock outputs the LMK04820 is able to distribute, then up to 15 differential clocks or 14 differential + 2 LVCMOS.

The following sections discuss specific features of the clock distribution channels that allow the user to control various aspects of the output clocks.

11.9.1 DCLKout DIVIDER

The device clocks (DCLKoutX), have a single clock output divider. The divider supports a divide range of 1 to 32 (even and odd) with 50% output duty cycle. The output of this divider may also be directed to the SDCLKoutY, where Y = X + 1.

11.9.2 SDCLKout DIVIDER

The SYSREF clocks (SDCLKoutY), all share a common divider. The divider supports a divide range of 8 to 8191 (even and odd).

11.9.3 DCLKout DELAY

The device clocks include both a analog and digital delay for phase adjustment of the clock outputs.

The analog delay allows a nominal 25 ps step size and range from 0 to 575 ps of total delay. Enabling the analog delay adds a nominal 500 ps of delay in addition to the programmed value.

The digital delay allows a group of outputs to be delayed from 4 to 32 VCO cycles. The delay step can be as small as half the period of the clock distribution path by using the DCLKoutX_HS bit. e.g. 2 GHz VCO frequency results in 250 ps coarse tuning steps. The coarse (digital) delay value takes effect on the clock outputs after a SYNC event. The half step bit takes effect immediately.

There are 2 different ways to use the digital delay.

1. Fixed Digital Delay — adjusts the clock output delays with a SYNC event.
2. Dynamic Digital Delay — adjusts the delay of a clock output with respect to other clocks operating without a SYNC event.

11.9.4 SDCLKout Delay

The SYSREF clocks include both an analog and digital delay for phase adjustment of the SYSREF clocks.

The analog delay allows for 150 ps steps and range from 1 to 2250 ps.

The digital delay allows the SYSREF output to be delayed from 0 to 10.5 VCO cycles. The delay step can be as small as half the period of the clock distribution path by using the DCLKoutX_HS bit. e.g. 2 GHz VCO frequency results in 250 ps coarse tuning steps. The digital delay value takes effect on the clock outputs after a SYNC event. The half step bit takes effect immediately.

11.9.5 GLITCHLESS HALF SHIFT and GLITCHLESS ANALOG DELAY

The device clocks also include a feature to ensure glitchless operation of the half shift and analog delay operations.

11.9.6 PROGRAMMABLE OUTPUT FORMATS

For increased flexibility all LMK04820 device and SYSREF clock outputs (DCLKoutX or SDCLKoutY) can be programmed to an LVDS, LVPECL, or HSDS output type. The OSCout can be programmed to an LVDS, LVPECL, or LVCMOS output type.

Any LVPECL output type can be programmed to 1600, or 2000 mVpp amplitude levels. The 2000 mVpp LVPECL output type is a Texas Instruments proprietary configuration that produces a 2000 mVpp differential swing for compatibility with many data converters and is also known as 2VPECL.

11.9.7 CLOCK OUTPUT SYNCHRONIZATION

Using the SYNC input causes all active clock outputs to share a rising edge.

The SYNC event also causes the digital delay values to take effect.

11.10 0-DELAY

The LMK04820 supports two types of 0-delay, either of which will work with internal or external VCO's.

1. Cascaded 0-delay
2. Nested 0-delay

Cascaded 0-delay mode synchronizes the phase of PLL2 input clock, OSCin, to the phase of the output clock. The 0-delay feedback may performed with an internal feedback loop from any of the clock groups or with an external feedback loop into the FBCLKin port as selected by the FB_MUX.

Nested 0-delay mode synchronizes the phase of the PLL1 input clock to the output clock phase. The 0-delay feedback may performed with an internal feedback loop from any of the clock groups or with an external feedback loop into the FBCLKin port as selected by the FB_MUX. In this mode CLKin, OSCin, and CLKout have deterministic phase relationships, but CLkin to CLKout phase will be less accurate than nested 0–delay mode.

Without using 0-delay mode there will be n possible fixed phase relationships from clock input to clock output depending on the clock output divide value and VCO frequency.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

11.11 STATUS PINS

The LMK04828 provides status pins which can be monitored for feedback or in some cases used for input depending upon device programming. For example:

- The CLKin_SEL0 pin may indicate the LOS (loss-of-signal) for CLKin0.
- The CLKin_SEL1 pin may be an input for selecting the active clock input.
- The Status_LD1 pin may indicate if the device is locked.
- The Status_LD2 pin may indicate if PLL2 is locked.

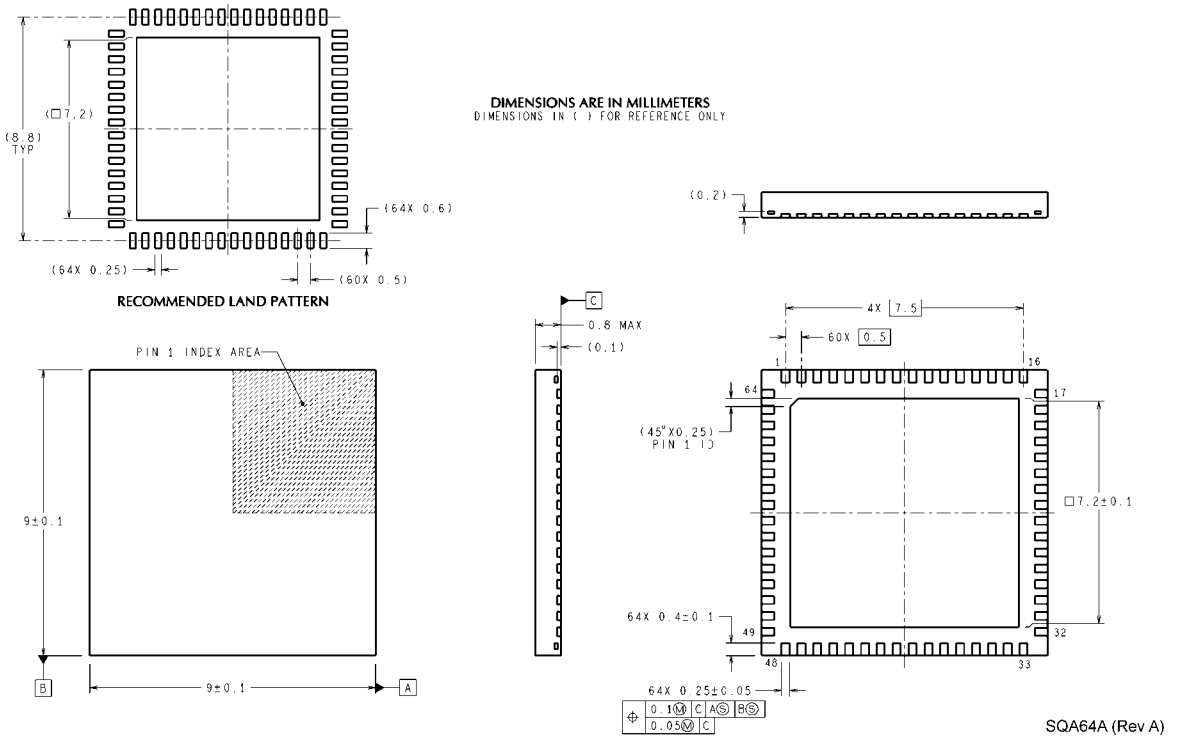
The status pins can be programmed to a variety of other outputs including analog lock detect, PLL divider outputs, combined PLL lock detect signals, PLL1 Vtune railing, readback, etc. Refer to the SPI programming section of this datasheet for more information.

11.12 SPI PROGRAMMING INTERFACE

Allows for writing and reading the device configuration.

Accepts a read/write bit + 15 address bits + 8 data bits.

12.0 Physical Dimensions inches (millimeters) unless otherwise noted



13.0 Ordering Information

Order Number	Ref Inputs	Buffered OSCin Outputs	Programmable Outputs	VCO	Packaging	Package Marking
LMK04828BISQE	2	1	14	2.5 and 2.9 GHz	250 Unit Tape and Reel	K4828
LMK04828BISQ					1000 Unit Tape and Reel	
LMK04828BISQX					2500 Unit Tape and Reel	
LMK04826BISQE				1.9 and 2.5 GHz	250 Unit Tape and Reel	K4826
LMK04826BISQ					1000 Unit Tape and Reel	
LMK04826BISQX					2500 Unit Tape and Reel	

Notes

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